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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,299	09/12/2003	Howard Hao Chen	YOR920030184US1(8728-625)	7457

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,299	CHEN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *31-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-30 and 60* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/12/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election with traverse of the Group I invention, claim(s) 1-30 and 60 in the response filed on April 25, 2005, is acknowledged. The traversal is on the ground(s) that "simultaneous examination of Group I and Group II will not present an undue burden...." This is not found persuasive.

A restriction requirement between one set of product claims and a set of process claims was issued in the Office action that was mailed on March 23, 2005. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct inventions,' which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." See *Applied Materials Inc. v. Advanced Semiconductor Materials* 40 USPQ2d 1481, 1492 (Fed. Cir 1996)(Archer, C.J., concurring in-part and dissenting in-part). A product and the process of making the product are "two independent, albeit related inventions." See *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See *In re Berg*, 46 USPQ2d 1226, 1233 n.10 (Fed. Cir. 1998).

The examiner, in issuing a restriction requirement, must demonstrate "one way distinctiveness." *Applied Materials Inc.* at 1492. As stated within the restriction requirement, "inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f))." In this application, the examiner restricted the product claims from the process claims on the grounds

that "the product as claimed can be made by another and materially different process such as a process wherein the device of Group I can be manufactured by forming plurality trenches in the semiconductor substrate by mechanical means, such as, imprinting instead of etching," and that, as a result, a restriction was necessary.

In addition to one way distinctiveness, the examiner must show "why it would be a burden to examine both sets of claims." *Applied Materials Inc.* at 1492. "A serious burden on the examiner may be *prima facie* shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803. An explanation was provided in the restriction requirement. Specifically, in addition to being distinct, the examiner indicated that restriction is proper because the product claims and the process claims "have acquired a separate status in the art."

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Accordingly, the restriction requirement in this application is still deemed proper and is therefore made FINAL.

2. Accordingly, claims 31-59 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention, the requirement having been traversed the response filed on April 25, 2005

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "**wherein the first continuous trench is formed in the horizontal direction,**" as recited in claim 27 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 5, 8-9, 17, 20, 27 and 28 are objected to because of the following informalities:

Claims 5, 8-9, 17, 20 and 28 contain improper Markush group of claims. It is improper to use the term "comprising" instead of "consisting of" See *Ex parte Dotter*, 12 USPQ 382 (Bd. App. 1931). Appropriate correction is required.

Claim 27 recites the limitation "wherein the first continuous trench is formed in the horizontal direction" in line 1-2. However, the recited limitation is not clear because the base claim recites forming of trench on the back side of the substrate and the trench

only can be vertically downward from the top-back surface. Therefore, it is not clear how the trench can be horizontal trench.

Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "stopping the etching of the semiconductor substrate when the dopant contained in the second diffusion layer is detected in a product of the etching" in lines 1-3. However, the recited limitation lacks clarity in the meaning and scope for the following reasons:

Does it mean the etching is stopped when the etchant reaches the second diffusion region?

Does it mean that the etching is stopped when the etchant removes the second diffusion region? And etc.

In addition it is not clear how the measurement is done in order to determine the detection of the product of etching.

Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Accordingly, claim 3 has not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection under 35 U.S.C. 103 should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 60 is rejected under 35 U.S.C. 102(e) as being anticipated by Eiles et al. (US/6,607,928).

Re claim 60, Eiles et al. disclose a method of forming cooling elements in a semiconductor substrate, comprising: etching the semiconductor substrate (204) from a backside of the semiconductor substrate (204) to form a plurality of trenches (240 242) (i.e., the openings 240 242); and depositing thermally conductive material (246 248) in the plurality of trenches (see Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1, 4, 5 and 7-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eiles et al. (US/6,607,929) in view of Hamburgen et al. (US/5,948,689).

Re claim 1, Eiles et al. disclose a method of forming cooling elements in a semiconductor substrate, comprising: etching the semiconductor substrate (204) from a backside of the semiconductor substrate (204) to form a plurality of trenches (240 242) (i.e., the openings 240

242); and depositing thermally conductive material (246 248) in the plurality of trenches (see Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25).

Although it is conventional to coat a mask layer on the substrate and to form a mask pattern in order to etch the substrate using the mask pattern as a mask, Eiles et al. do not specifically disclose coating a backside of the semiconductor substrate with a first mask layer forming a plurality of trench patterns in the first mask layer.

Hamburgen et al. disclose coating a backside of the semiconductor substrate (110) (see Figs. 1 and 3) with a first mask layer (251) forming a plurality of trench patterns (not shown) in the first mask layer (251); etching the semiconductor substrate (110) to form a plurality of trenches along the plurality of trench patterns (see Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50). As Hamburgen et al. disclose the well-known lithographic process used to form a trench by using a mask pattern.

One of ordinary skill in the art would have been motivated to coat a mask on a surface of the substrate and to pattern the mask in order to from a trench in the substrate using the mask pattern as a mask.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Eiles et al. reference with coating a backside of the semiconductor substrate with a first mask layer and forming a plurality of trench patterns in the first mask layer as taught by Hamburgen et al. because the well-known lithographic process is used to form a trench by using a mask pattern.

Re claim 4, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the first mask layer is a

photoresist (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 5, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the trench patterns are formed by one of optical, x-ray, extreme ultra-violet, electron beam and ion beam lithographic techniques (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Claim 7, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the plurality of trenches are formed in the vertical direction (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 8, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the step of depositing thermally conductive material is performed by one of chemical vapor deposition, atomic layer deposition, physical vapor deposition and electroplating (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 9, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the thermally conductive material is made from one of aluminum nitride, aluminum, copper-tungsten, silicon

carbide**, gold, copper, diamond and silver** (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 10, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the semiconductor substrate is one of a complimentary metal oxide semiconductor wafer and a silicon-on-insulator wafer (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 11, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the plurality of trenches are

formed in an intergrated-circuit chip of the semiconductor substrate. (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 12, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the step of etching the semiconductor substrate to form the plurality of trenches is performed away from at least one of a passivation layer, an interconnect layer, a device layer and a doped well structure of the semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 13, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the plurality of trenches are formed one of before and after processing of remaining portions of the semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 14, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation integrating an external heat sink (230) on the backside of the semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 15, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation integrating an active cooling apparatus (230) on the backside of the semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 16, as applied to claim 15 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the step of integrating the active cooling apparatus on the backside of the semiconductor substrate includes: coating the backside of the semiconductor substrate with a second mask layer; patterning the second mask layer; etching a continuous trench into the backside of the semiconductor substrate; forming at least one opening in the continuous trench for allowing coolant supplied from the active cooling apparatus to one of exit and enter the continuous

trench; and positioning the active cooling apparatus on the backside of the semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 17, as applied to claim 15 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the active cooling apparatus is one of a thermal electric cooling component, a micro-fan device and a micropump (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 18, as applied to claim 1 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the active cooling apparatus is one of directly fabricated on the backside of the semiconductor substrate and separately built and mounted on the backside of the semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 19, Eiles et al. disclose a method of forming an active cooling apparatus on a semiconductor substrate, comprising: etching a first continuous trench into the backside of the first semiconductor substrate; forming at least one opening in the first continuous trench for allowing coolant supplied from the active cooling apparatus to one of exit and enter the first continuous trench; and positioning the active cooling apparatus on the backside of the first semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25).

Although it is conventional to coat a mask layer on the substrate and to form a mask pattern in order to etch the substrate using the mask pattern as a mask to form a trench, Eiles et al. do not specifically disclose coating a backside of the semiconductor substrate with a first mask layer forming a plurality of trench patterns in the first mask layer.

Hamburgen et al. disclose coating a backside of the semiconductor substrate (110) (see Figs. 1 and 3) with a first mask layer (251) forming a plurality of trench patterns (not shown) in the first mask layer (251); etching the semiconductor substrate (110) to form a plurality of trenches along the plurality of trench patterns (see Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50). As Hamburgen et al. disclose the well-known lithographic process used to form a trench by using a mask pattern.

One of ordinary skill in the art would have been motivated to coat a mask on a surface of the substrate and to pattern the mask in order to from a trench in the substrate using the mask pattern as a mask.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Eiles et al. reference with coating a backside of the semiconductor substrate with a first mask layer and forming a plurality of trench patterns in the first mask layer as taught by Hamburgen et al. because the well-known lithographic process is used to form a trench by using a mask pattern.

Re claim 20, as applied to claim 19 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the active cooling apparatus is one of a thermal electric cooling component, a micro-fan device and a

micropump (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 21, as applied to claim 19 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the active cooling apparatus is one of directly fabricated on the backside of the first semiconductor substrate and separately built and mounted on the backside of the first semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 22, as applied to claim 19 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including forming a second semiconductor substrate including a second continuous trench; and fastening the second semiconductor substrate to the first semiconductor substrate at a position between the backside of the first semiconductor substrate and the active cooling apparatus, whereby the active cooling apparatus rests on the second semiconductor substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 23, as applied to claim 22 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the second continuous trench is a mirror image of the first continuous trench of the first substrate (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

24. The method as recited in claim 22, wherein the step of fastening includes

one of anodic bonding and metallurgical soldering (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 25, as applied to claim 22 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the second semiconductor substrate includes at least one opening in the second continuous trench for allowing the coolant supplied from the active cooling apparatus to one of exit and enter the second continuous trench (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 26, as applied to claim 19 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the mask layer is a photoresist (see Eiles et al. Figs. 2 and 3 and related text in Col. 2, line - Col. 4, line 25; Hamburgen et al. Figs. 1 and 3 and related text in Col. 2m line 55 – Col. 4, line 50).

Re claim 27, as applied to claim 19 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the first continuous trench is formed in the horizontal direction.

Re claim 28, as applied to claim 19 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the first semiconductor substrate is one of a complimentary metal oxide semiconductor wafer and a silicon-on-insulator wafer.

Re claim 29, as applied to claim 22 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the second semiconductor substrate is one of a silicon substrate and a plate-glass substrate.

Re claim 30, as applied to claim 19 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including the limitation wherein the first continuous trench is formed in an intergrated-circuit chip of the first semiconductor substrate.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eiles et al. (US/6,607,929) in view of Hamburgen et al. (US/5,948,689), as applied in Paragraph 10 above, and further in view of Wolf, *Silicon Processing for the VLSI Era Volume 2-Process Integration*, pp 51-54, 1990.

Re claim 6, as applied to claim 1 in Paragraph 10 above, Eiles et al. and Hamburgen et al. in combination disclose all the claimed limitations including using of fluorine based plasma the etch the semiconductor.

However both Eiles et al. and Hamburgen et al. silent about the use of chlorine based plasma to etch the substrate during formation of the trench.

Wolf discloses the conventional chlorine based etchant to form deep trench in the substrate (see Wolf Pages 51-54). Wolf discloses, chorine based etch gases produced a good trench-wall profiles (see Wolf Page 53).

One of ordinary skill in the art would have been motivated to use chlorine based plasma to from a trench in order to obtain good trench-wall profile.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Eiles et al. and Hamburgen et al. chlorine based plasma etch gas as taught by Wolf. in order to obtain good trench-wall profile.

Allowable Subject Matter

12. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Nakanishi et al. (US/5,403,783) and Hanari et al. (US/5,532,906) also disclose similar inventive subject matter.

Correspondence

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Examiner
Art Unit 2823

BK
May 12, 2005